In the Specification:

Please amend paragraph 0063 on page 17 as follows:

Other methods and variations of forming a structure are disclosed in co-pending application Serial No. 10/729,095, filed December 5, 2003[[_____ (TSM03-0615)]], which is incorporated herein by reference. The methods and variations taught in that application can be applied to the structures disclosed herein. For the sake of simplicity, each of these variations will not be repeated herein.

Please amend paragraph 0050 on page 14 as follows:

Figure 6a shows a gate stack 412 formed in the first and second active regions 408/410. The gate stack 412 may comprise a hard mask 418, a gate electrode 204 and a gate dielectric 206. A hard mask 418 forms a protective layer on the top of the gate electrode 204. The gate electrode 204 overlies the gate dielectric 206. The gate dielectric 206 is formed using any gate dielectric formation process known and used in the art, e.g., thermal oxidation, nitridation, sputter deposition, or chemical vapor deposition. The physical thickness of the gate dielectric 206 may be in the range of about 5 to about 100 angstroms. The gate dielectric 206 may employ a conventional gate dielectric such as silicon oxide and silicon oxynitride or a high permittivity (high-k) gate dielectric, or combinations thereof. The formation of the gate stack 412 applies to both PMOS transistors and NMOS transistors, and the width of the gate of a PMOS transistor and the width of the gate of an NMOS transistor are preferably related. In the preferred embodiment, the ratio of the width of the gate of the PMOS transistor to a width of the gate of the NMOS transistor is approximately equal to the square root of a ratio of electron mobility to the hole mobility in the channel region. In alternative embodiments, the preferred ratio is approximately equal to the ratio of electron mobility to hole mobility in the channel region.